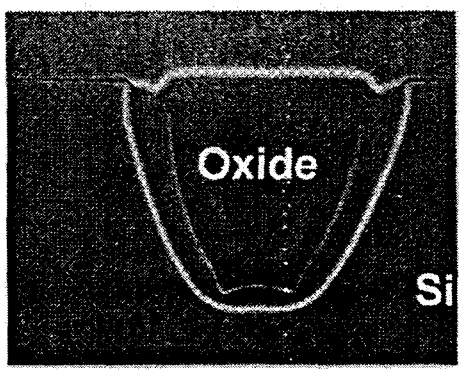
Overview

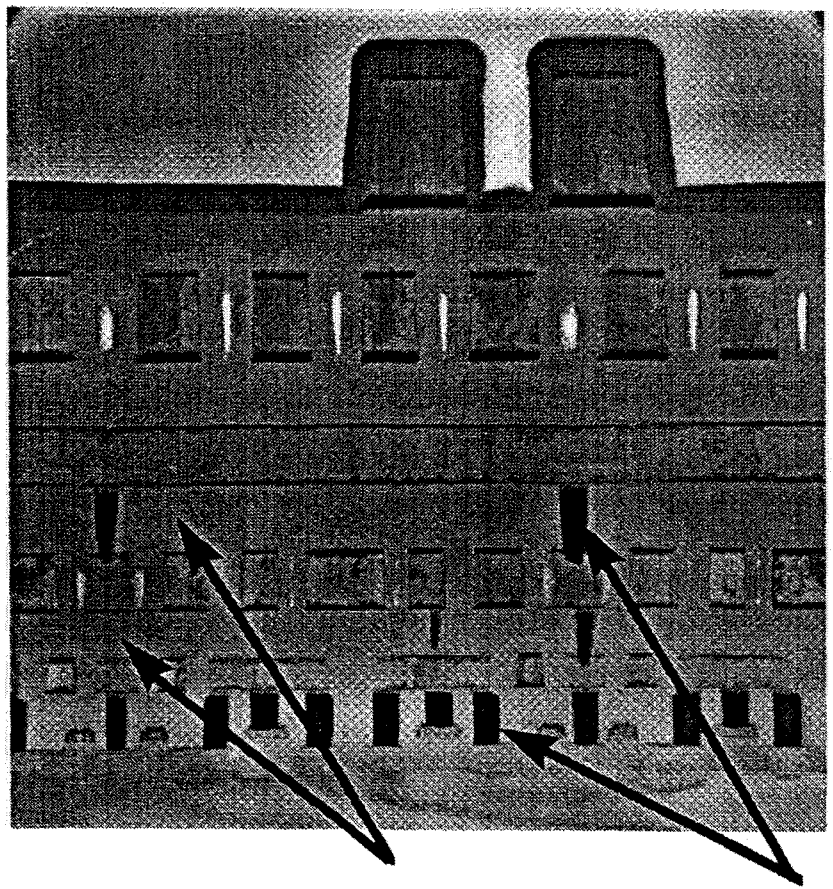
Third Implementation P6 Family Microprocessor:

- 5-Layer Metal 0.25μ CMOS Process Technology
- 450 MHz Clock Rate
- Full Intel Instruction Set Including MMX™ Instructions
- Mobile, Desktop, and 4-Way MP Server Support
- Wide Voltage Operation (1.6V to 2.0V Nominal)
- L2 Cache Support at Half and Full Core Clock Frequency
- C4 and Wire Bond Technologies

Cross-section of 0.25µ Technology

Shallow Trench Isolation





M5
(2.56µ Pitch)

M4
(1.6µ Pitch)

M3
(0.93µ Pitch)

M2
(0.93µ Pitch

M1
(0.64µ Pitch

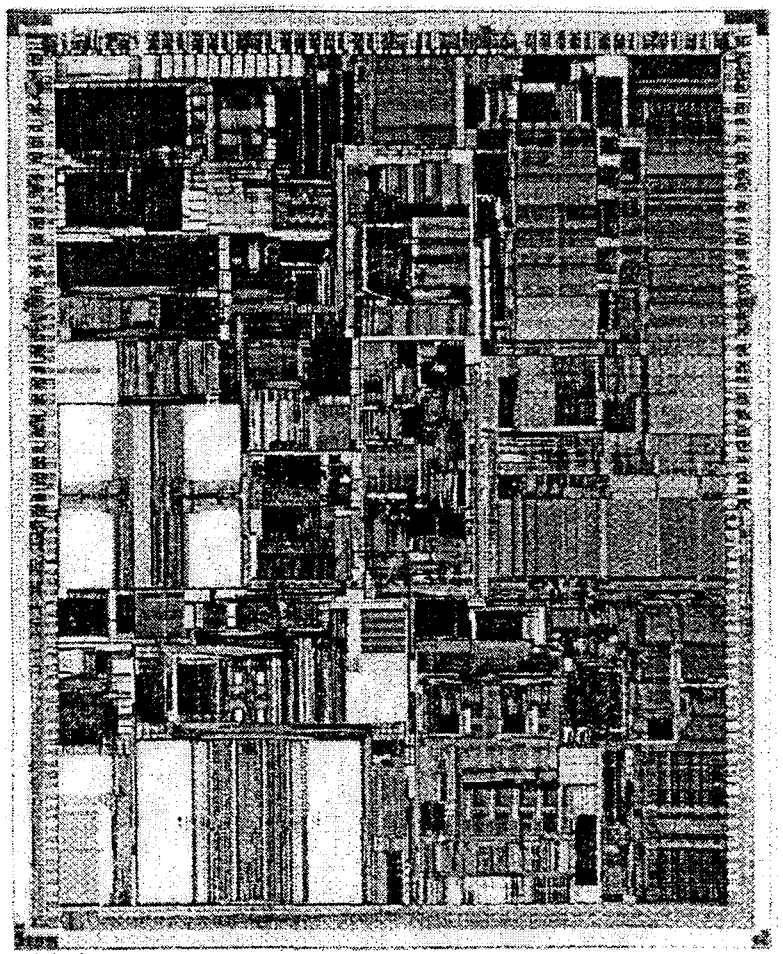
Dielectric (Oxide)

Tungsten Plugs

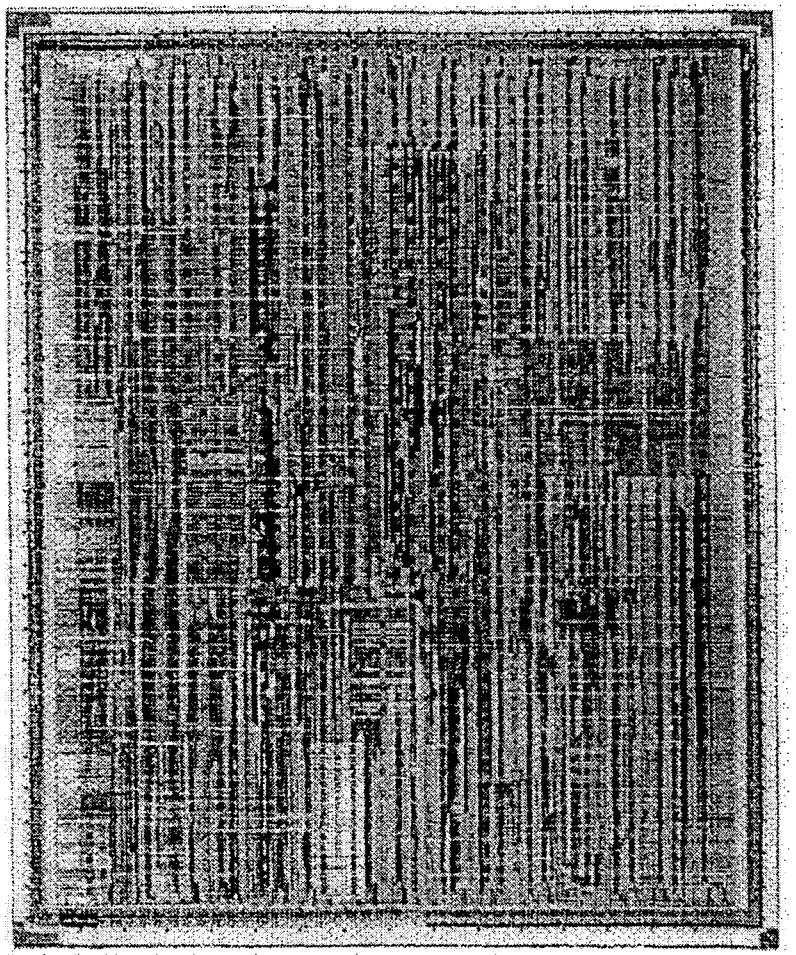
Metal 5 Usage

- RC Delay Reduction
- Area Reduction
- Support Use of C4 Bumps

Processor Die Photos



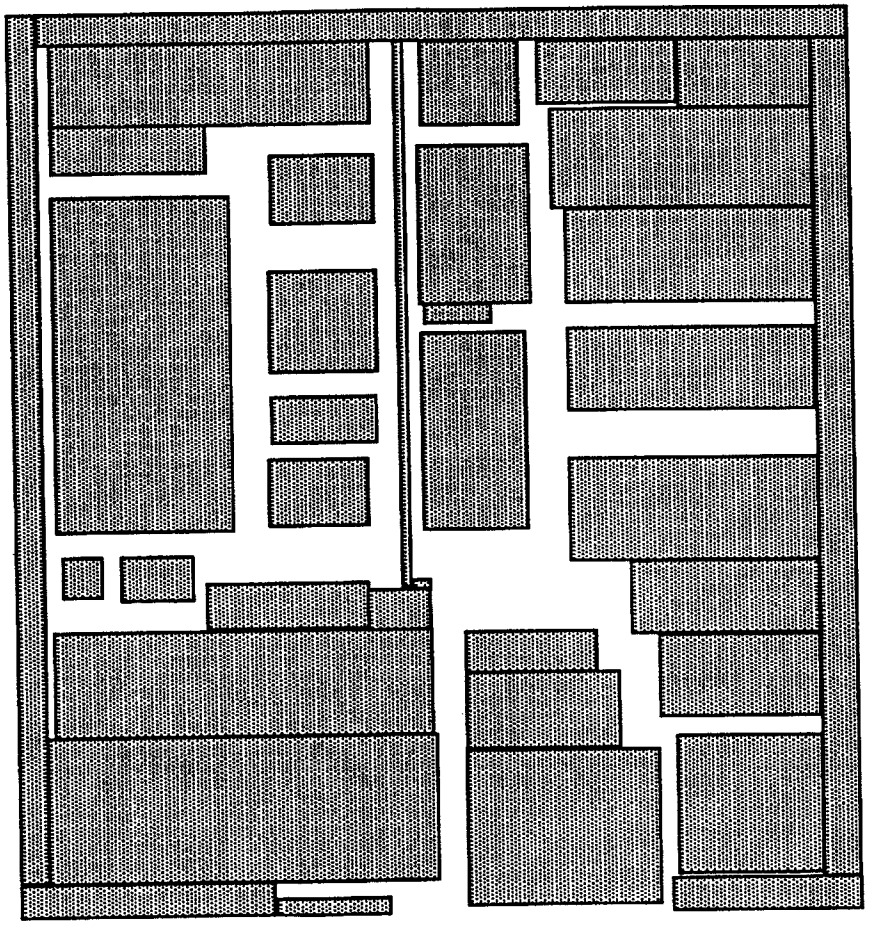
Die After M3



Die Processed Through C4 And Subsequently Stripped Back To M4

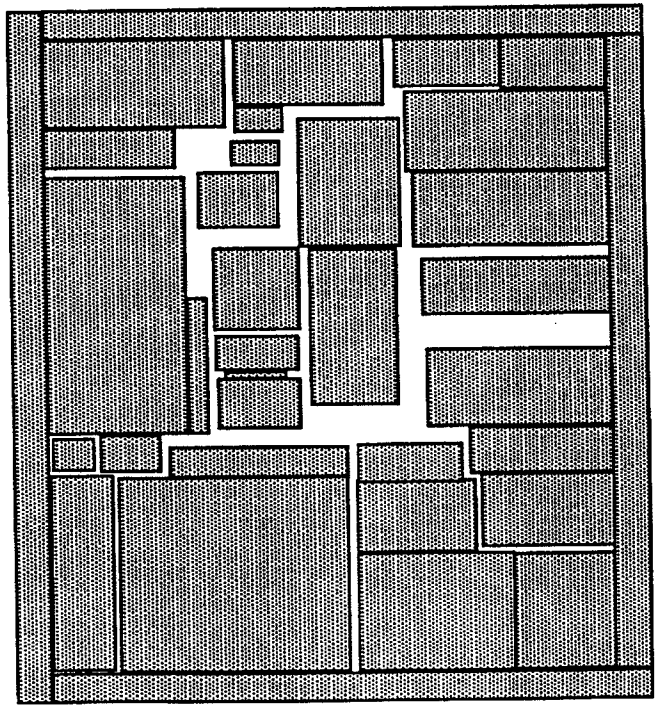
Reduction of Routing Channel Area

0.35μ Design



203 (mm^2)

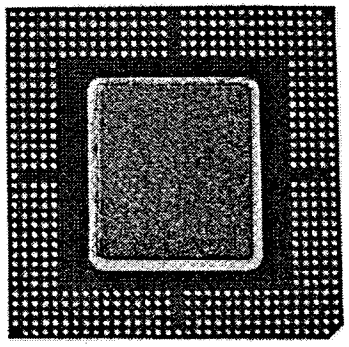
0.25μ Design



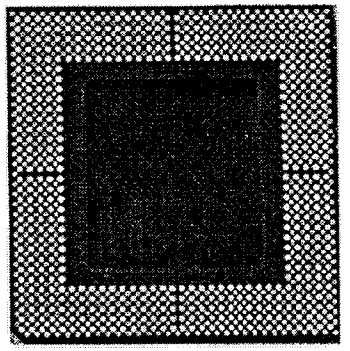
131 (mm^2)

Packaging

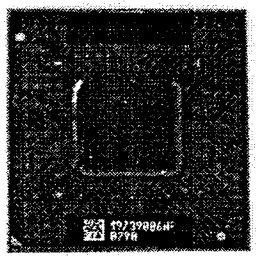
- Die Supports Both Wire Bond and C4 Package Types
- Wire Bond Package:
  - Plastic Land Grid Array
  - 42.5 mm Square
  - 68 μ Pad Pitch
- C4 Package:
  - Organic Land Grid Array
  - 31 mm Square
  - 245 μ Bump Pitch
- 120 nF On Die Bypass Capacitance Eliminates Capacitors in Package

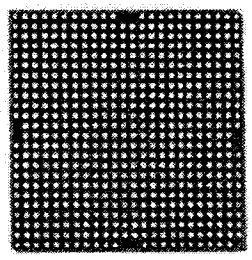


(TOP)

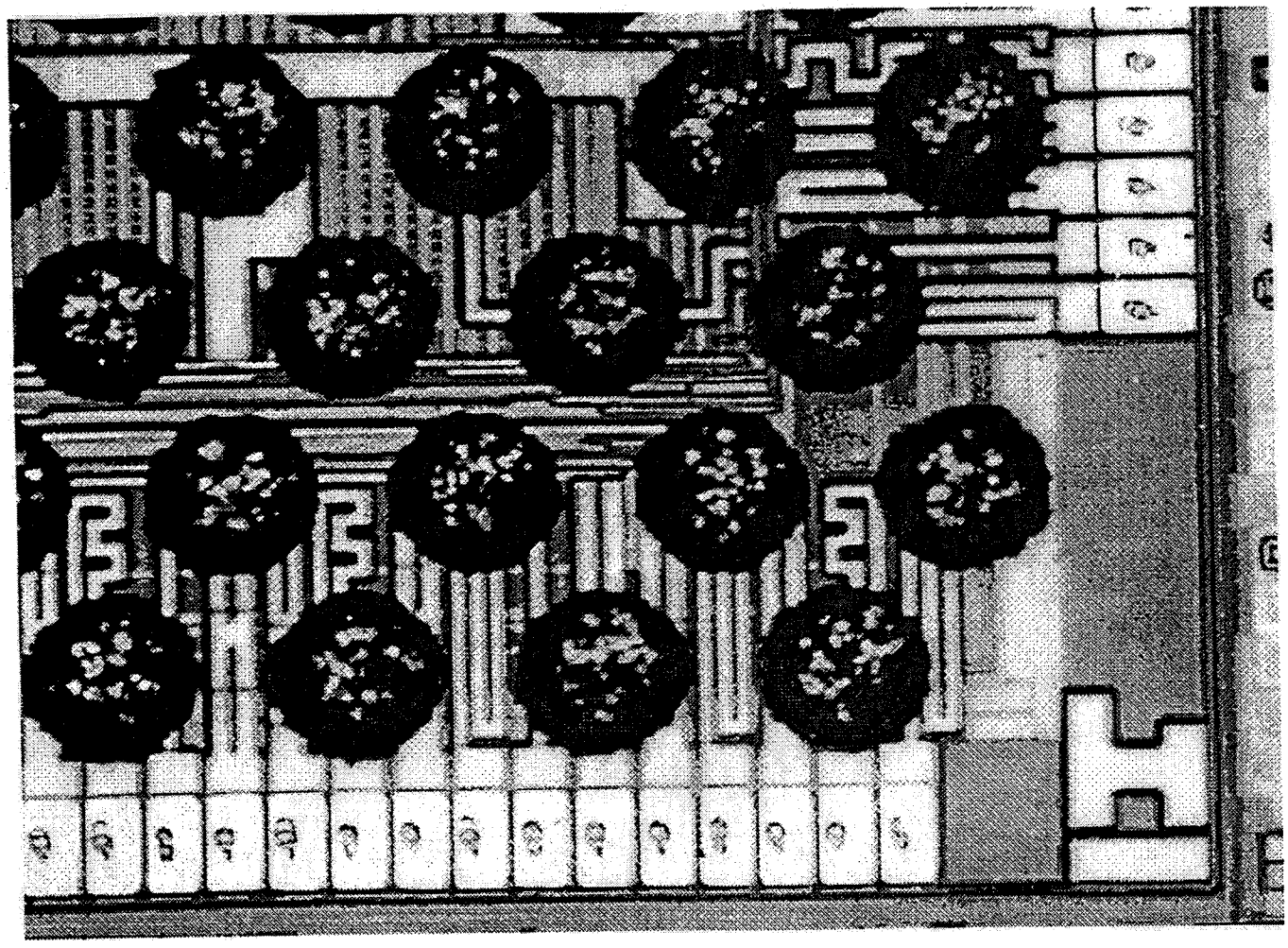


(BOTTOM)





Wire Bond Pads and C4 Bumps



Design Challenges

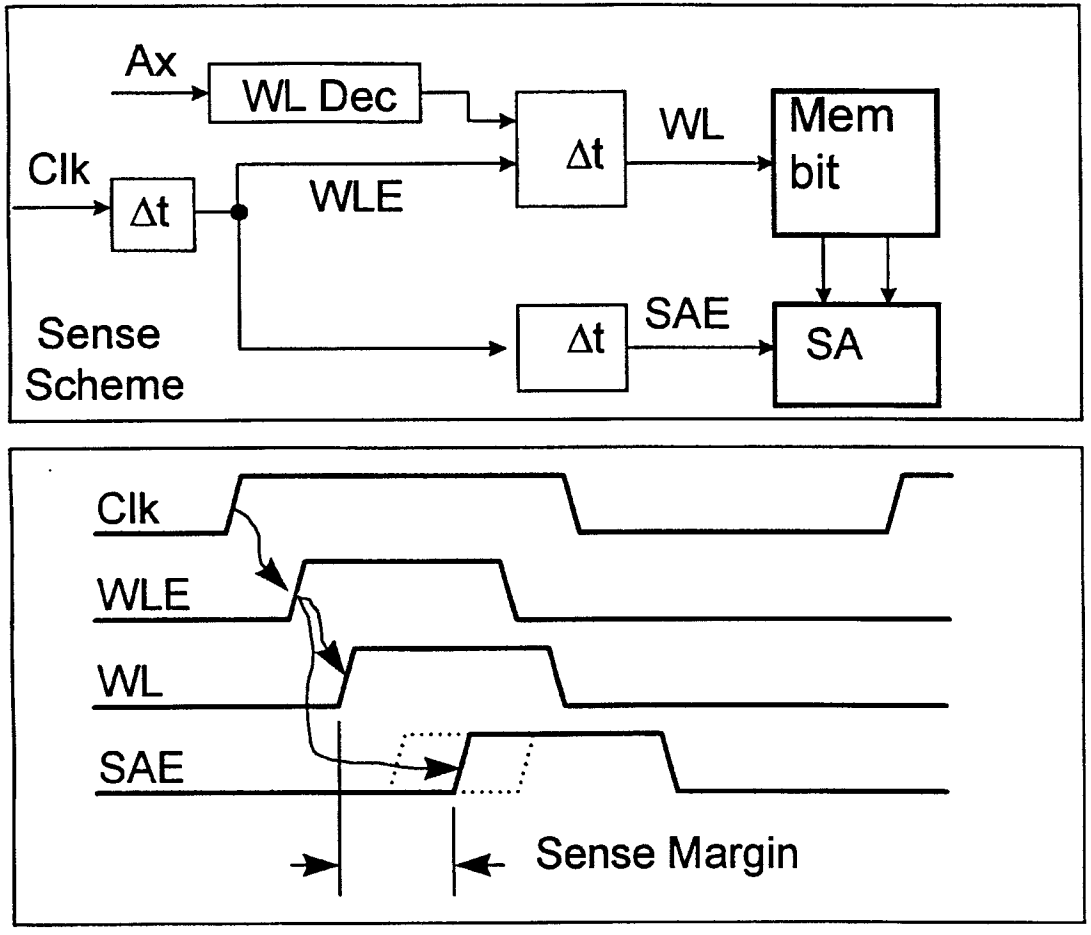
➢ Short Design Cycle

- Silicon Process Technology Demands
  - Line-to-Line Coupling
  - Spatial Variation
- Product Demands
  - High Speed Off Die Busses
  - Voltage Operating Range

Short Design Cycle

- Datapath Circuits Linearly Shrunk
- Caches, I/O, & Analog Redesigned to 0.25μ Rules
- Control Blocks Redesigned With Auto Place and Route
- Chip Re-routed Over The Circuit Blocks

Programmable Cache Array Timers

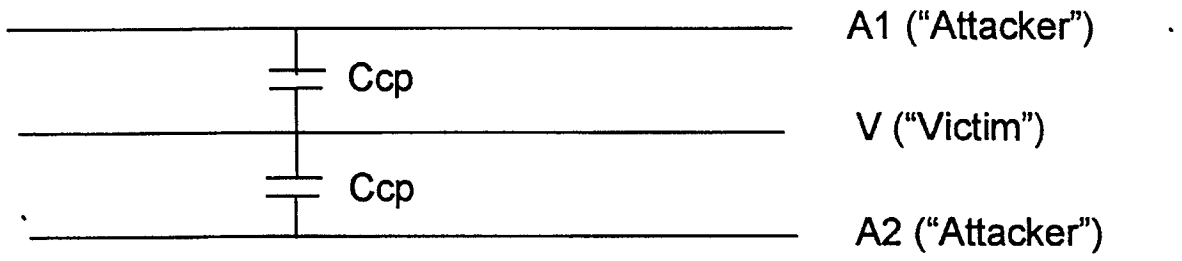


- Delays Critical Timing To Cache Circuits
- Rapid Characterization And Margin Testing in Mfg
- Independent Settings For 1.6V And 2.0V Operation
- 10 Arrays: 0.3% Die Area Cost

Design Challenges

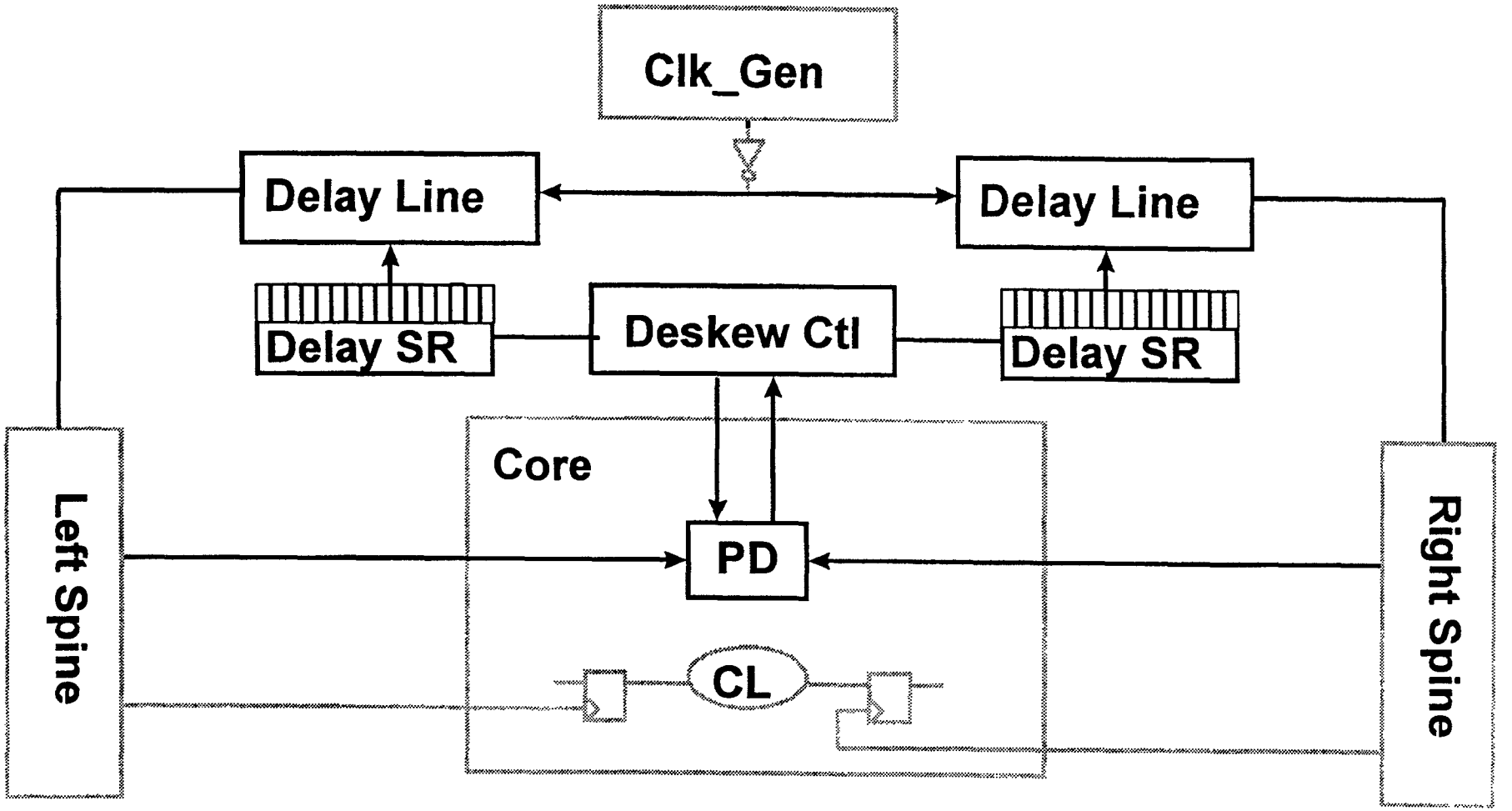
- Short Design Cycle
- **Silicon Process Technology Demands**
  - **Line-to-Line Coupling**
  - **Spatial Variation**
- Product Demands
  - High Speed Off Die Busses
  - Voltage Operating Range

Line-To-Line Signal Coupling



- Historically Ccp Modeled As Terminating At AC Ground
- If Signals A1 and A2 Are Switching Effect on V Increased
- Design Methodology:
  - Ccp Determined Through RC Extraction
  - Static Timing Run Determines Slope of A1, A2
  - Second Static Timing Run Determines Effect On V
- Layout Techniques Useful To Correct Impact:
  - Increase Spacing
  - Interleave With Signals That Switch In Different Clocks

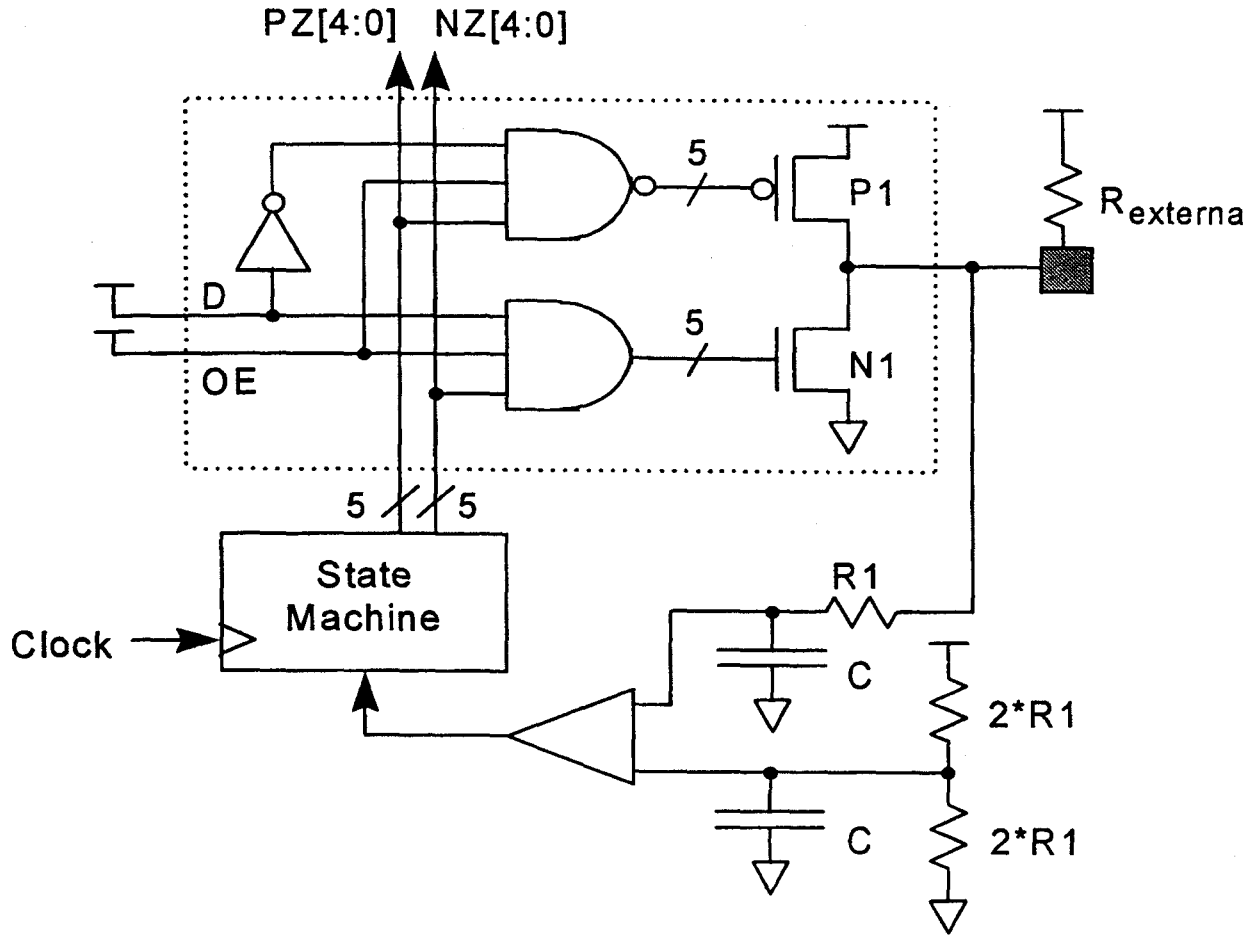
Clock Deskewing Circuit



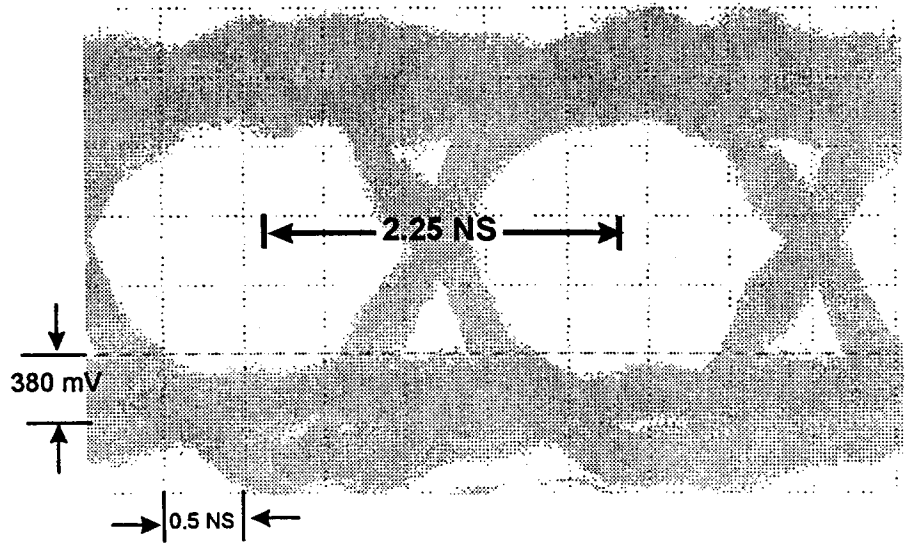
Design Challenges

- Short Design Cycle
- Silicon Process Technology Demands
  - Line-to-Line Coupling
  - Spatial Variation
- **Product Demands**
  - **High Speed Off Die Busses**
  - **Wide Voltage Operating Range**

Backside Bus Impedance Control Circuit

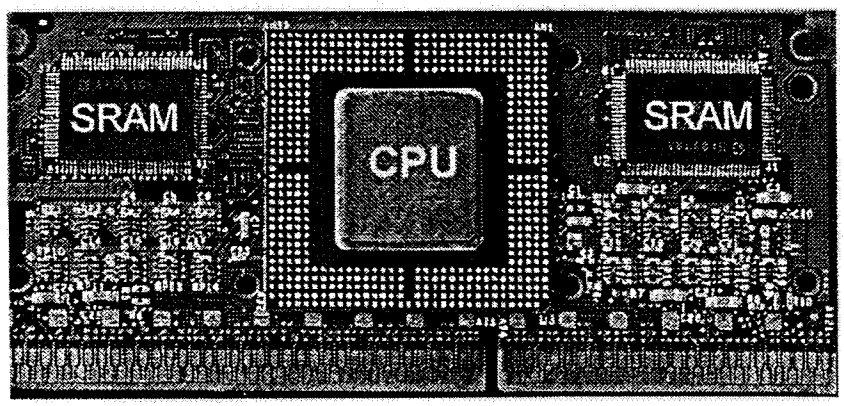


Backside Bus Waveforms With 450 MHz Core Clock

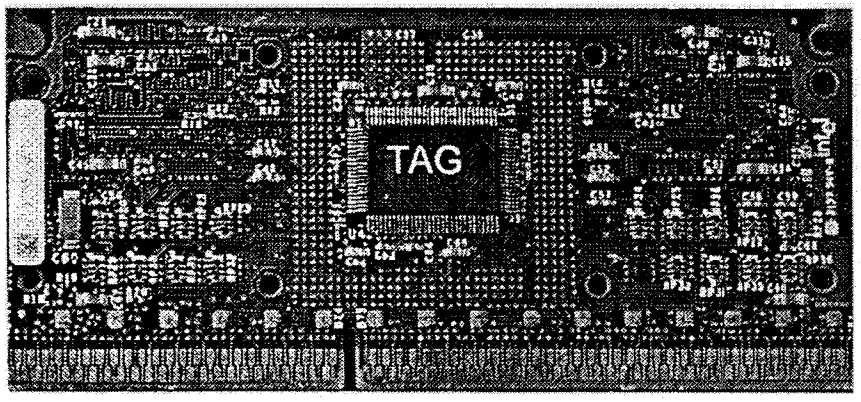


Pentium®II Processor "Slot 1" Substrate

- 512K Pipelined Burst SRAM (2x256K)
- Data Transfers At 0.5X Core Clock Rate



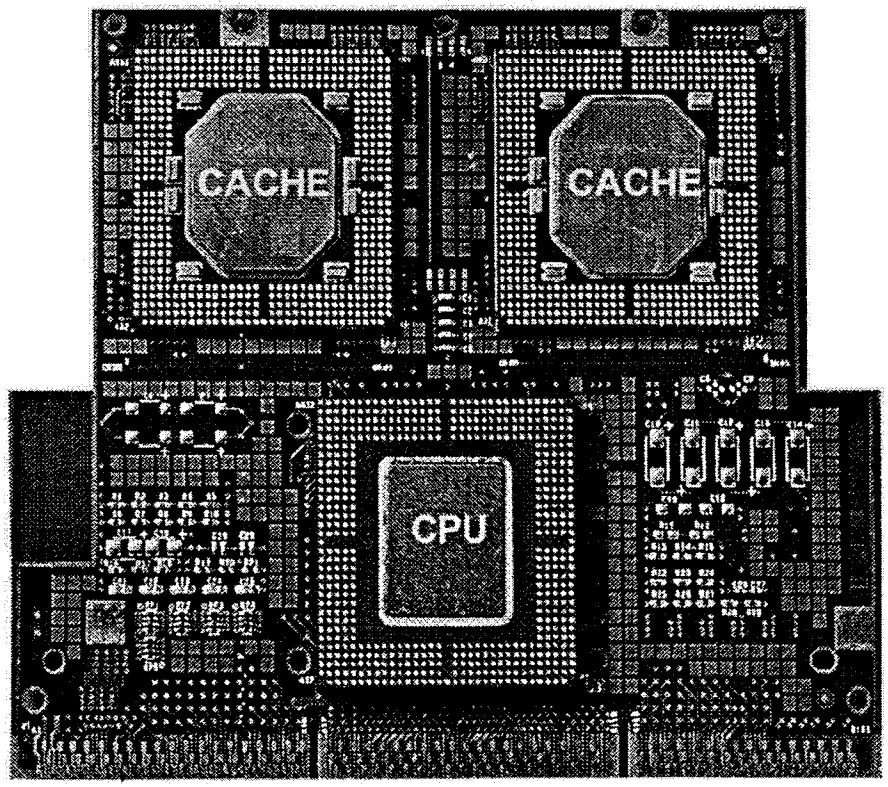
Top View



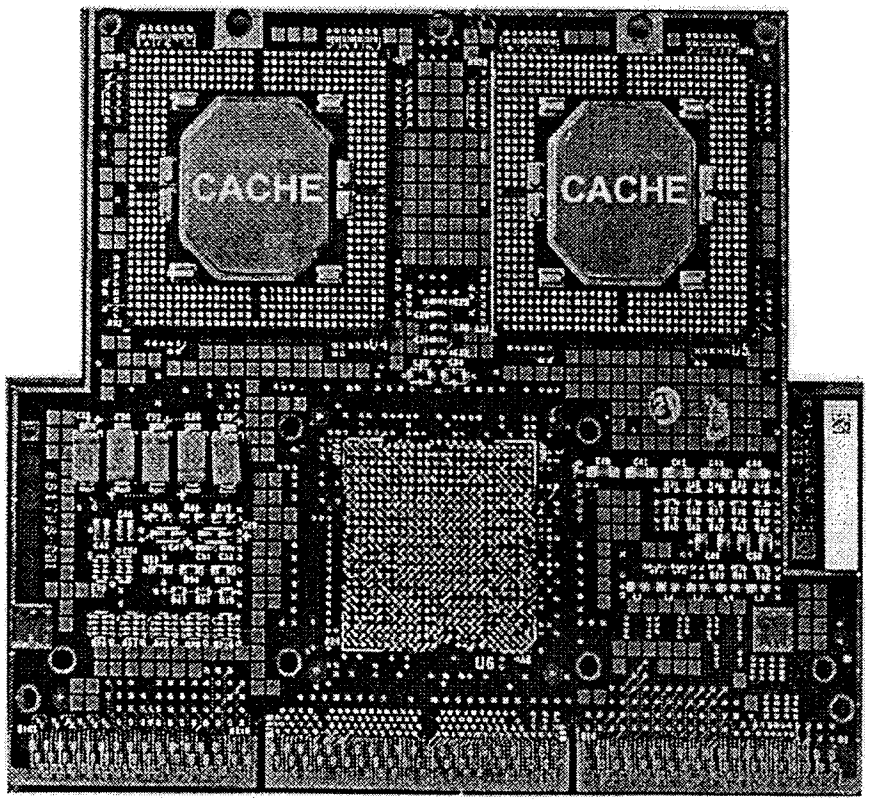
Bottom View

"Slot 2" Server Substrate

- 2 MB Custom Cache RAM (4x512K)
- Data Transfers At Full Clock Rate

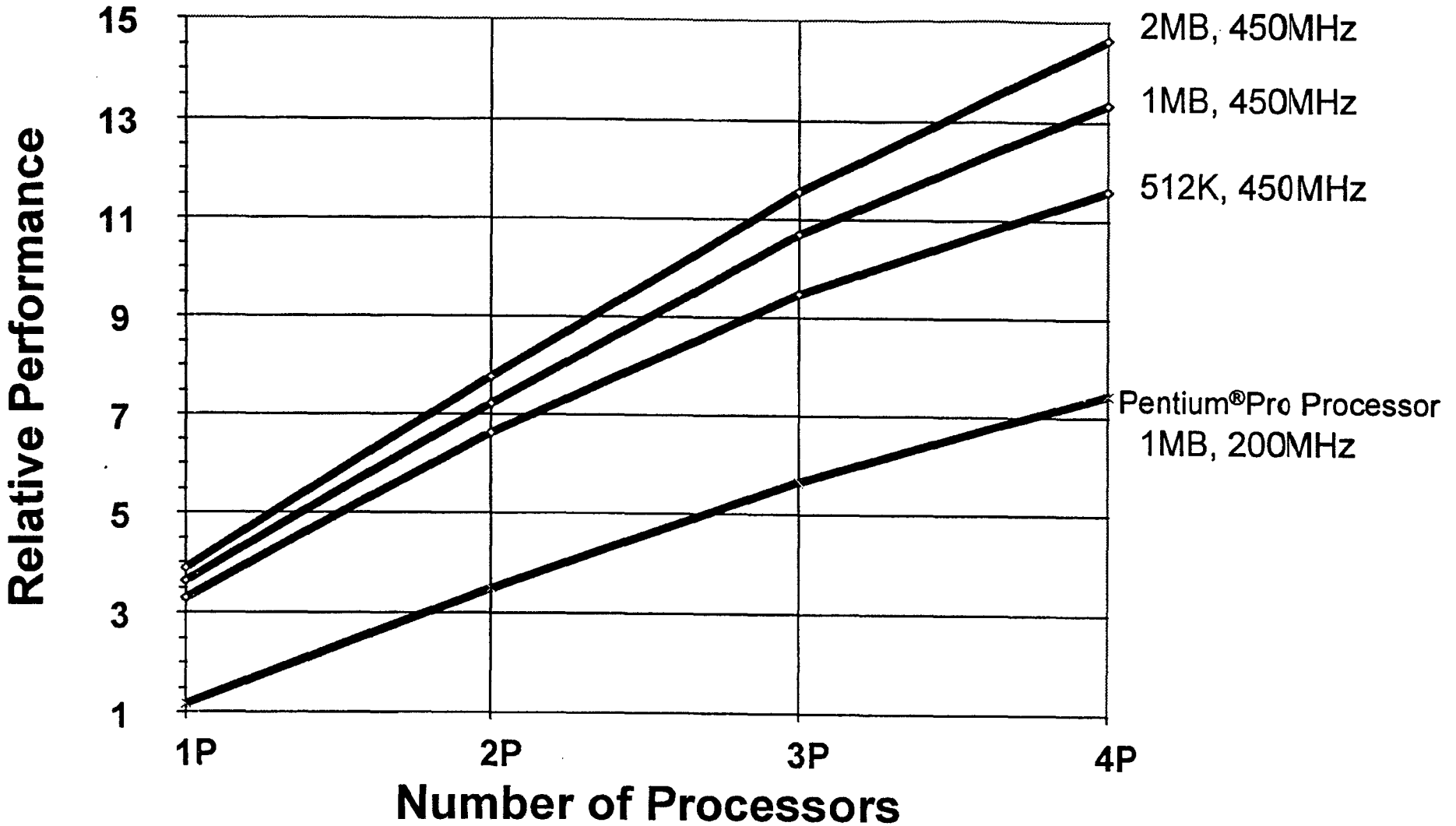


Top View

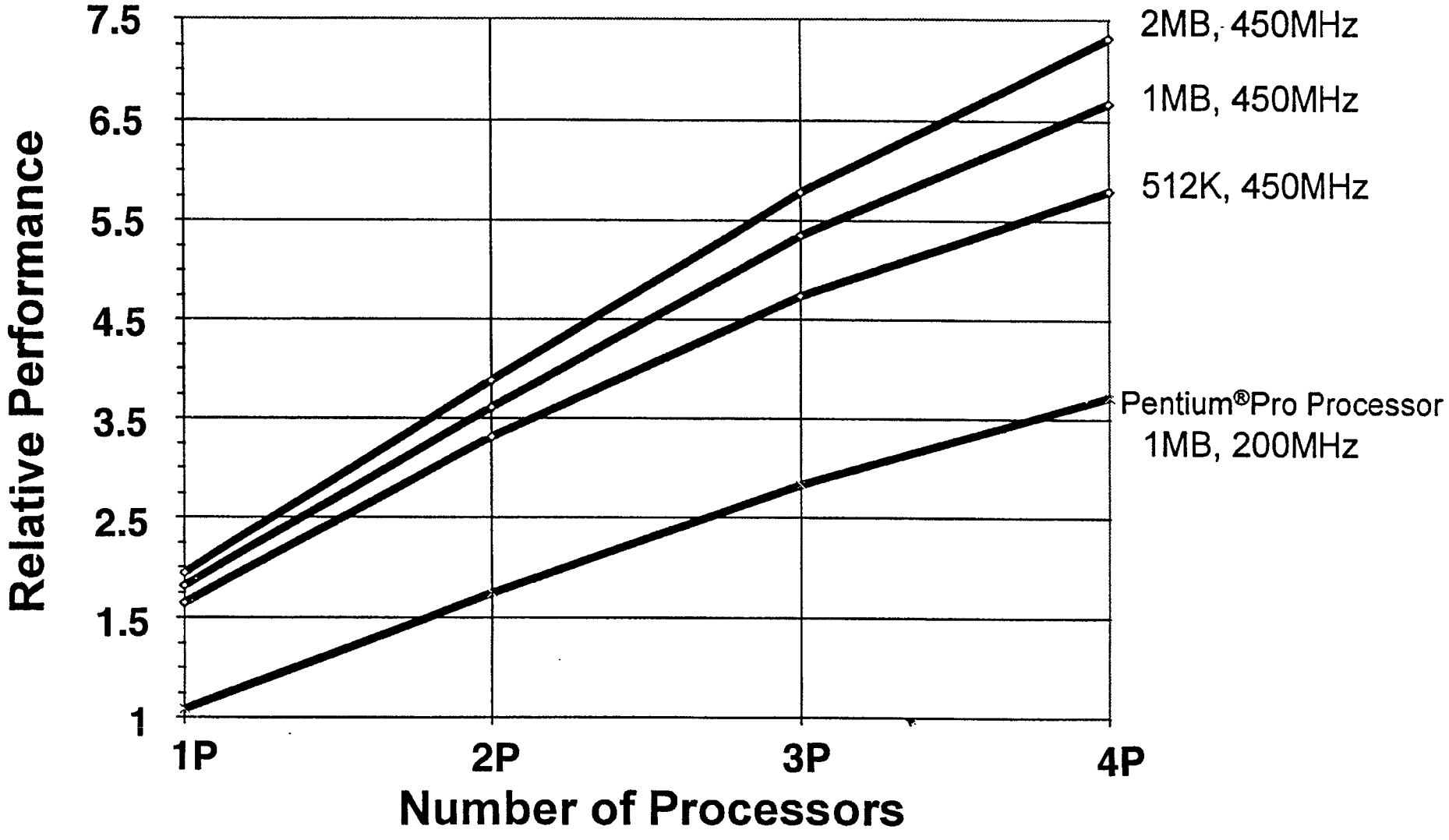


Bottom View

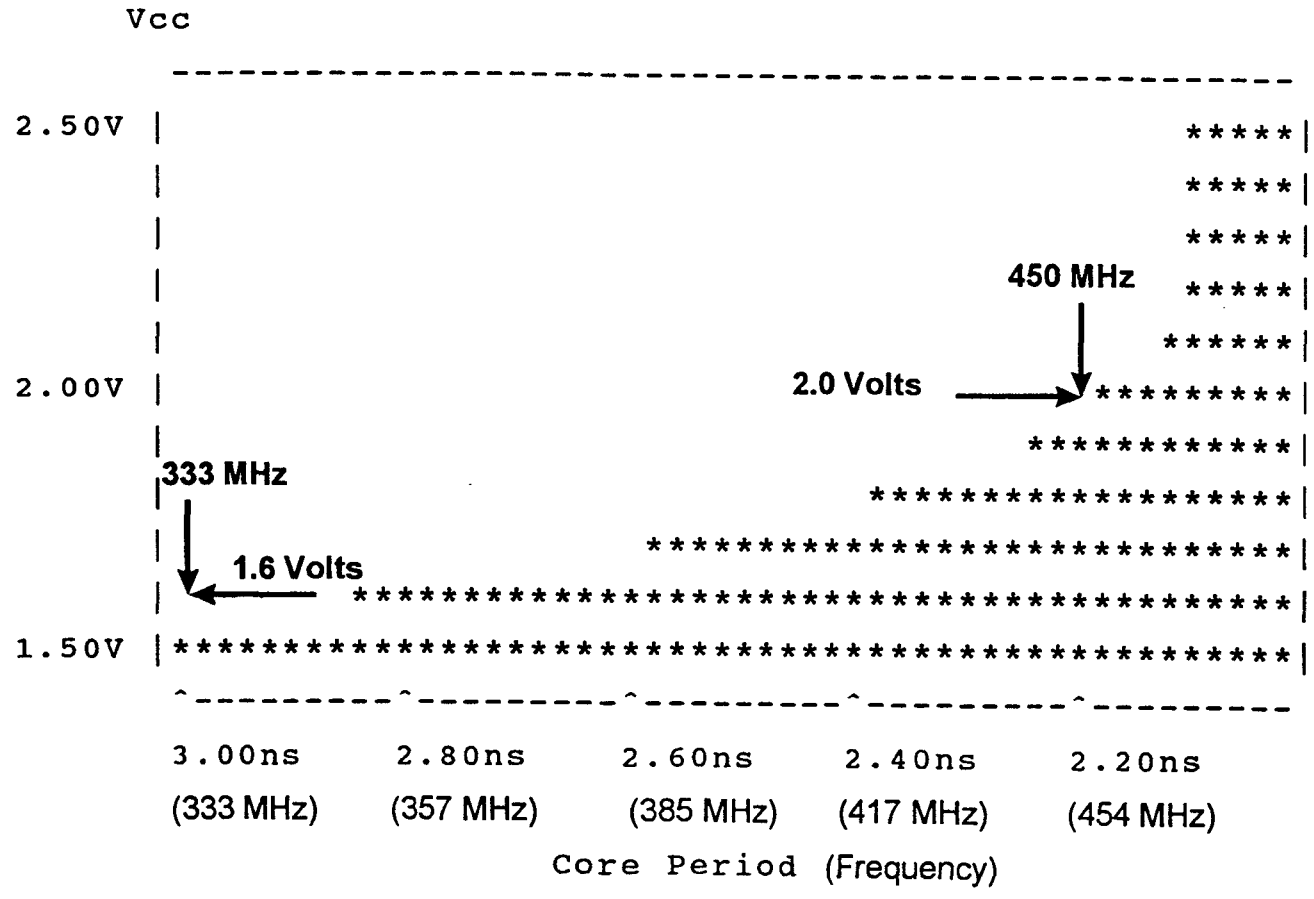
MP Performance



MP Performance



Shmoo Demonstrating 450 MHz Operation*



Summary

A Third Implimentation P6 Family Microprocessor Has Been Described Which:

- Is Manufactured On An Advanced 0.25μ CMOS Process Technology
- Operates At Frequencies Up To 450 MHz For Desktop and Server Applications
- Provides Power Consumption of Less Than ~8 Watts For Mobile Applications